UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/804,554	03/12/2001	Donald Henry Willis	PU010053	1285

7590 07/31/2003

Joseph S. Tripoli
THOMSON multimedia Licensing Inc.
Patent Operations,
P.O. Box 5312, Two independence Way
Princeton, NJ 08543-5312

EXAMINER
NATNAEL, PAULOS M

ART UNIT	PAPER NUMBER
.2614	

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/804,554	WILLIS, DONALD HENRY	
	Examiner	Art Unit	
	Paulos M. Natnael	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Mar. 19, 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-24 and 26-31* is/are rejected.

7)☒ Claim(s) *3,10,18,19 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims **1,2,4-9,11-17,20-24, 26-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuji et al. U.S. Pat. No. 5,111,297.

Claim **1** is a method claim of claim **14**, and therefore, Claim 1 is rejected for the same reasons as claim 14.

Considering claim **2**,

a) supplying a plurality of delayed output video signals, is met by frame Memory 22, fig.6;

b) speeding up each of said plurality of delayed video signals to said first and second faster line rates, and sequentially supplying all of said speeded up video signals for said writing step, is met by the disclosure that line memory 23 "produces an output signal which is the interpolated scanning line video signal b of the previous line."(col. 6, lines 8-9)

Considering claim **4**, the method of claim 1, comprising the step of writing said lines to a liquid crystal on silicon display.

Regarding claim 4, see rejection of claim 14 (f).

Considering claim **5**, the method of claim 1, comprising the step of propagating said input video signal through a memory embedded in an integrated circuit;

Regarding claim 5, the Examiner takes official notice in that integrated circuitry is well known in the art and therefore would have been obvious to the skilled at the time the invention was made to modify the system of Tsuji and include the memory in an integrated circuit in order to reduce cost or conserve space and make the circuit compact.

Considering claim **6**, the method of claim 1, comprising the step of propagating said input video signal through just enough memory to delay said input video signal by fn-1)/n of said frame period, where n is a multiplication factor of said frame multiplying, is met by the second Frame memory 22, fig.6;

Considering claim **7**, the method of claim 1, comprising the steps of: at least doubling said frame rate of said input video signal; and, writing each of said lines multiple times to said liquid crystal display, is met by the disclosure that the system "performs a double

scanning conversion, thereby providing a sub-picture without causing line flicker." (See Abstract)

Considering claim **8**, the method of claim 1, comprising the step of speeding up said delayed video signal and said input video signal to the same line rate faster than fHin.

Claim **9**, is a method claim of claim 14, and therefore, Claim 9 is rejected for the same reasons as claim 14.

Considering claim **11**, the method of claim 9, comprising the step of 2 writing said lines to a liquid crystal on silicon display.

Regarding claim 11, see rejection of claim 14(f).

Considering claim **12,** the method of claim 9, comprising the step of 2 propagating said input video signal through a memory embedded 3 in an integrated circuit.

Regarding claim 12, see rejection of claim 5.

Considering claim **13**, the method of claim 9, comprising the step of 2 speeding up said delayed video signal and said input video signal to the same line rate of 2fHin.

Regarding claim 13, see rejection of claim 7.

Considering claim **14**,

a) a first memory for said input video signal, said first memory having a maximum required data storage capacity just large enough to delay said input video signal for a fraction of a frame period 1/fvin, is met by Second Frame Memory 22, Fig.6;

b) a second memory for speeding up said delayed video signal to a first line rate faster than fHin, is met by Line Memory 23, fig.6;

c) a third memory for speeding up said input video signal to a second line rate faster than fHin, is met by the first frame memory 21, fig.6;

d) a multiplexer coupled for receiving both said speeded up video signals and supplying said speeded up video signals one line at a time for writing to ...a display, is met by second selection circuit 26, fig.6;

e) a source of clock signals and control signals, said source being coupled to each of said memories, to said multiplexer and to said liquid crystal display, such that successive lines supplied by said multiplexer to said liquid crystal display originate alternately from said second and third memories at said faster line rates, at least some of said supplied lines being supplied to said liquid crystal display multiple times within

each said frame period, is met by Frame synchronizing circuit 4, Fig.6, and by the disclosure "a control means which controls (1) read out, from the first and second memory means, either the same field-basis signal twice or the frame-basis signal, and (2) output of the signal read out from the first memory means as the sub-picture video signal for the main scanning line and the signal read out of the second memory means as the sub-picture video signal for the interpolated scanning line". (col.2, line 67 thru col. 3, line 6)

Except for;

f) the claimed liquid crystal display;

Regarding f), Tsuji et al. Does not specifically disclose an LCD display. Tsuji discloses a television receiver. However, Examiner takes Official Notice in that the LCD display is well known in the art, and it would have been obvious to the skilled in the art to modify the system of Tsuji et al. by providing an LCD display to display the television signals on the LCD monitor, in order to make the system more versatile and useful to the user, because Tsuji's output form the second selection circuit intended to use any well known type of display.

Considering claim **15**, the frame rate multiplier of claim 14, wherein said maximum required data storage capacity of said first memory is (n-1)/n of a frame, where n is the multiplication factor of said frame rate multiplier.

Regarding claim 15, Tsuji does not specify how large the memories are. However, it would have been obvious matter of design choice to modify the Tsuji reference by having a first memory that is ½ of a frame or 2/3, ¾ or, 4/5 of a frame, etc. since applicant has not disclosed that having such size difference solve any stated problem or is for any particular purpose and it appears that any other memory would perform equally well.

Considering claim **16**, the frame rate multiplier of claim 15, wherein said first memory has n-1 outputs for supplying n-1 delayed output video signals, where n > or = 2, is met by the Second Frame memory 22, fig.6;

Considering Claim **17**, the frame rate multiplier of claim 16, comprising:
n-1 memories coupled to said first memory and to said multiplexer for speeding up said n-1 delayed output video signals to said faster line rates; and, said lines supplied by said multiplexer to said liquid crystal display originating sequentially from said third memory and said n-1 memories, is met by line memory 23, fig.6, which is coupled to Frame Memory 22 and "produces an output signal which is the interpolated scanning line video signal b of the previous line." (col. 6, lines 8-9)

Considering Claim **20**, the frame rate multiplier of claim 14, wherein said first and second memories are functionally combined into a single memory to both delay and speed up said input video signal.

Regarding claim 20, making separate item integral by functionally combining them is not patentable. (See In re Larson, 144 USPQ 347 (CCPA 1965); see also In Lockhart, 90 USPQ 214 (CCPA 1951))

Considering Claim **21**, the frame rate multiplier of claim 14, wherein said first, second and third memories are functionally combined into a single memory to delay and speed up said delayed input video signal and to speed up said input video signal.

Regarding claim 21, see rejection of claim 20;

Considering claim **22**, the frame rate multiplier of claim 14, wherein said first and second faster line rates are the same.

Regarding claim 22, Tsuji does not specify whether the first and second line rates are the same; However, it would have been obvious matter of design choice to modify the Tsuji reference by having the two line rates the same since applicant has not disclosed that having them the same solves any stated problem or is for any particular purpose and it appears that any line rate would perform equally well.

Considering claim **23**, see rejection of claim 14.

Considering claim **24**, the frame rate doubler of claim 23, wherein said first memory has a maximum required data storage capacity of 1/2 of a frame.

Regarding claim 24, see rejection of claim 15;

Considering claim **26**, the frame rate doubler of claim 23, wherein said liquid crystal display comprises liquid crystal on silicon.

Regarding claim 26, see rejection of claim 11;

Considering claim **27**. The frame rate doubler of claim 23, wherein said frame rate doubler is at least partly formed integrally in an integrated circuit.

Regarding claim 27, see rejection of claim 12;

Considering claim **28**, the frame rate doubler of claim 27, wherein said first memory is formed integrally in said integrated circuit.

Regarding claim 28, see rejection of claim 12;

Considering claim **29**, the frame rate doubler of claim 23, wherein said first and second memories are functionally combined into a single memory to both delay and speed up said input video signal.

Regarding claim 29, see rejection of claim 20;

Considering claim **30**, the frame rate multiplier of claim 23, wherein said first, second and third memories are: functionally combined into a single memory to delay and speed up said delayed input video signal and to speed up said input video signal.

Regarding claim 30, see rejection of claim 21;

Considering claim **31**, the frame rate multiplier of claim 23, wherein said first and second faster line rates are the same.

Regarding claim 31, see rejection of claim 22;

Allowable Subject Matter

3. Claims **3,10, 18, 19 and 25** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to disclose a frame rate doubler, wherein the source of clock signals and control signals provides an operating mode in which a multiplexer is controlled to: periodically interrupt said supply of said lines to said liquid crystal display; supply to said liquid crystal display during said periodic interruptions n successive lines from said second memory or n successive lines from said third memory; and, alternately

select said n successive lines from said second or third memory in order to maintain a uniform time interval between writing lines into the same line-number position on said liquid crystal display, as in claims 18 and 25;

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Faroudja et al. U.S. Pat. No. 5,159,451 discloses a field memory expansible line doubler for television receiver.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paulos M. Natnael whose telephone number is (703) 305-0019. The examiner can normally be reached on 6:30am -3pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller can be reached on (703) 305-4795. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-4750.

MICHAEL H. LEE
PRIMARY EXAMINER

Paulos Natnael

July 25, 2003

pmn